Application N.E. 19/814,306

AMENDMENT TO CLAIMS

ntly amended) A simulator apparatus comprising:

a <u>plurality of simulator [[model]] models each</u> including a functional model for <u>a CPU</u> constituting a system to be simulated;

a simulator model including a functional model for hardware to be connected to buses linked to the <u>corresponding CPU</u>;

plural types of interfaces included in the simulator models and enabling plural types of simulators for various uses to access to the functional models; and

a simulator controlling device for selecting any of the plural types of the interfaces and accessing the respective functional models via the selected interfaces.

- (Original) A simulator apparatus as claimed in Claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying software.
- 3. (Original) A simulator apparatus as claimed in Claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying hardware.
- 4. (Original) A simulator apparatus as claimed in Claim 1, wherein the interfaces for the respective functional models comprise an interface usable in a simulator for verifying a system.

Application No.: 10/814,306

- (Original) A simulator apparatus as claimed in Claim 1, wherein the interfaces for the respective functional models comprise an interface usable in debugging.
- 6. (Currently amended) A simulator apparatus as claimed in Claim 1, wherein an interface capable of simulating clock cycles of the system as precision at processing to perform precise simulation for the system at clock level is comprised.
 - 7. (Cancelled)
- 8. (Original) A simulator apparatus as claimed in Claim 1, wherein the interfaces for the respective functional models comprise an interface for extension usable in performance analysis.